IN THE CLAIMS

1. (Original) A method comprising:

providing a semiconductor wafer having a plurality of integrated circuit dice formed therein, the integrated circuit dice including a plurality of electrically conductive contact pads and electrically conductive trim pads exposed on an active surface of the wafer;

forming contact bumps on a plurality of the contact pads;

probing the wafer after the contact bumps have been formed, wherein the wafer probing includes,

a trimming operation that includes probing the plurality of electrically conductive trim pads and trimming circuits associated with the trims pads as necessary, and

a testing operation that involves probing at least some of the plurality of contact bumps to test selected functionalities of the integrated circuits; and

applying an electrically insulative undercoating to the active surface of the wafer that directly covers the trim pads while leaving at least portions of the contact bumps exposed, the undercoating being applied after the wafer probing, whereby the wafer may be trimmed and tested at substantially the same stage of wafer processing.

2. (Original) A method as recited in claim 1 wherein the probing for the trimming and testing operations is performed sequentially.

3. (Original) A method as recited in claim 1 wherein the probing for the trimming and testing operations are performed substantially simultaneously.

4. (Original) A method as recited in claim 1 wherein the undercoating is formed from a material selected from the group consisting of: epoxies, polyimides, and silicone-polyimide copolymers.

5. (Original) A method as recited in claim 1 wherein the undercoating has a final thickness in the range of approximately 0.2 and 4 mils.

6. (Original) A method as recited in claim 1 wherein the undercoating is formed from an underfill material that is suitable for filling a region between a die and a substrate that the die is mounted to after the wafer has been diced and the die mounted to the substrate.

7. (Original) A method as recited in claim 1 wherein the undercoating is formed from a B-stageable material.

8. (Original) A method as recited in claim 1 wherein the undercoating is formed from a curable material, the method further comprising curing the undercoating to permanently affix the undercoating to the surface of the wafer.

9. (Original) A method as recited in claim 1 wherein the undercoating is applied by one of a spin-on coating process, a molding process, a screen printing process and a stencil printing process.

10. (Original) A packaged integrated circuit device comprising:

a die having a plurality of electrically conductive contact pads on an active surface of the die and at least one electrically conductive trim pad on the active surface;

a plurality of contact bumps, each contact bump being formed on an associated contact pad; and

an undercoating adhesive adhered directly to the active surface of the die, the undercoating adhesive being arranged to cover, electrically isolate and directly adhere to the trim pads.

11. (Original) A semiconductor wafer comprising:

a plurality of semiconductor dice, each die having a plurality of electrically conductive contact pads on an active surface of the wafer wherein at least some of the electrically conductive contact pads have contact bumps formed thereon, each die further including at least one electrically conductive trim pad;

an undercoating adhesive adhered directly to the active surface of the wafer, the undercoating adhesive being arranged to cover, electrically isolate and directly adhere to the trim pads.

12. (Original) The semiconductor wafer of claim 11 herein the undercoating adhesive layer is optically transparent or translucent.

~~14~~ 13. (Currently Amended) The semiconductor wafer of claim 11 wherein the undercoating adhesive layer is selected from the group comprising: epoxies, polyimides, or silicone-polyimide copolymers.

14. (Original) The semiconductor wafer of claim 11 wherein the undercoating layer has a thickness in the range of approximately 0.2 to 4 mils.

15. (Original) The semiconductor wafer of claim 11 wherein the electrically conductive trim pads are formed from a material selected from the group consisting of aluminum, nickel, gold, copper, titanium, palladium, silver, chromium, tungsten and vanadium and alloys thereof.